



# **Intel® Xeon® Processor E5- 1600/E5-2600/E5-4600 v2 Product Families**

**Boundary Scan Descriptor Language (BSDL) Readme**

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*July 2014*



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## Revision History

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Document Number	Revision Number	Description	Date
329190	001	<ul style="list-style-type: none"><li>Initial Release</li></ul>	September 2013
329190	002	<ul style="list-style-type: none"><li>Intel® Xeon® Processor E5-4600 Product Family Release</li><li>Removed Reset Sequence diagram, no longer applicable</li></ul>	March 2014
329190	003	<ul style="list-style-type: none"><li>Intel® Xeon® Processor E5-4600 Product Family Release</li><li>Removed Reset Sequence diagram, no longer applicable</li></ul>	July 2014

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# Overview

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## Scope

This document is intended for the development of IEEE 1149 Boundary scan tests for the Intel® Xeon® Processor E5-1600 v2/E5-2600/E5-4600 v2 Product Families. This readme assumes a working knowledge of IEEE 1149 methodologies and the in circuit test (ICT) manufacturing test methods.

## Related Documents

Refer to the following documents for additional processor information.

**Table 1. Related Documents**

Document	Document Number/Location
Intel® Xeon® Processor E5-1600/E5-2600/E5-4600 v2 Product Families - EDS Volume 1	<a href="http://www.intel.com">http://www.intel.com</a>
Intel® Xeon® Processor E5-1600/E5-2600/E5-4600 v2 Product Families Specification Update	<a href="http://www.intel.com">http://www.intel.com</a>
IEEE Standard Test Access Port and Boundary Scan Architecture Specification	<a href="http://standards.ieee.org">http://standards.ieee.org</a>



### 1. Partial Boundary Scan File Needed with Limited BCLK Cycles.

**Workaround:** A workaround to this is to enable Partial Boundary-scan functionality. If a continuous BCLK[1:0] cannot be supplied, BSCAN functionality can still be enabled with the exception of the DDR pins. To enable this mode, a full initialization sequence must be applied prior to any BSCAN operation. 1000 BCLK cycles must be applied from assertion of PWRGOOD.

- a. `DRAM_PWR_OK_C[1/23]`, `PWRGOOD`, `RESET_N` are initialized LOW.
- b. `DRAM_PWR_OK_C[1/23]` `PWRGOOD` pins must be driven HIGH 2ms after power pins are stable and remain driven HIGH during the boundary-scan test pattern execution.
- c. Start 1000 BCLK cycles.
- d. Apply `IVB_EP_BSCAN_INIT.TXT` sequence.
- e. `RESET_N` pin should be driven LOW for the duration of pattern execution.

- Load 9 bit IR with 0x054.
- Load 146 bit DR with 0x00080000000000000000000000000000

See [Figure 1](#) for an example test flow.

**Figure 1. Test Flow with Partial BSCAN Initialization Example**



