Non-Planar, Multi-Gate InGaAs Quantum Well Field Effect Transistors with High-K Gate Dielectric and Ultra-Scaled Gate-to-Drain/Gate-to-Source Separation for Low Power Logic Applications

M. Radosavljevic, G. Dewey, J. M. Fastenau*, J. Kavalieros, R. Kotlyar, B. Chu-Kung, W. K. Liu*, D. Lubyshev*, M. Metz, K. Millard, N. Mukherjee, L. Pan, R. Pillarisetty, W. Rachmady, U. Shah, and Robert Chau

Intel Corporation, Technology and Manufacturing Group, Hillsboro, OR 97124, USA

* IQE Inc, Bethlehem, PA 18015, USA

Contact: robert.s.chau@intel.com

Abstract

In this work, non-planar, multi-gate InGaAs quantum well field effect transistors (QWFETs) with high-K gate dielectric and ultra-scaled gate-to-drain and gate-to-source separations (L_{SIDE}) of 5nm are reported for the first time. The high-K gate dielectric formed on this non-planar device structure has the expected thin T_{OXE} of 20.5Å with low J_G, and high quality gate dielectric interface. The simplified S/D scheme is needed for the non-planar architecture while achieving significant reduction in parasitic resistance. Compared to the planar high-K InGaAs QWFET with similar T_{OXE}, the non-planar, multi-gate InGaAs QWFET shows significantly improved electrostatics due to better gate control. The results of this work show that non-planar, multi-gate device architecture is an effective way to improve the scalability of III-V QWFETs for low power logic applications.

Introduction

Non-planar, multi-gate architectures have been investigated for improved electrostatics in Si MOSFETs [1], and most recently in III-V MOSFETs [2]. In this work, non-planar, multi-gate InGaAs QWFETs with high-K gate dielectric and ultra-scaled L_{SIDE} of 5nm are reported. These non-planar, multi-gate QWFET devices have undoped InGaAs channel in the shape of a "fin" formed on top of large band gap InAlAs barrier, with simplified n^{++} InGaAs source/drain scheme. Compared to the planar high-K InGaAs QWFET with similar electrical oxide thickness (T_{OXE}), the non-planar, multi-gate QWFET devices in this work show (i) more enhancement-mode threshold voltage (V_T) and (ii) significantly improved electrostatics with reducing transistor gate length (L_G) due to stronger gate control of the channel. In addition, the ultra-scaled L_{SIDE} combined with the simplified n^{++} InGaAs source/drain (S/D) scheme will enable device footprint scaling.

III-V QWFET Evolution from Planar to Non-planar

Figs. 1(a)-(d) show the progression of InGaAs QWFET from planar Schottky gate device to non-planar, multi-gate architecture with high-K gate dielectrics suitable for low power logic. Fig. 1(a) shows the planar Schottky gate QWFET with S/D comprised of n^{++} InGaAs cap, thick upper barriers and Si δ-doping [3]. In Fig. 1(b) the planar QWFET structure is similar to Fig. 1(a) except that the Schottky gate is replaced by high-K gate stack to reduce both T_{OXE} and gate leakage (J_G) [4]. In this work, the thick upper barriers and Si δ-doping are removed in the S/D area of Fig. 1(b), thus simplifying the S/D scheme as shown in the device in Fig. 1(c). Eliminating the thick upper barriers and Si δ-doping while using n^{++} InGaAs cap as the carrier supply enables S/D contact area scaling with low resistance [5]. Finally Fig. 1(d) shows the non-planar, multi-gate high-K QWFET with the ultra-scaled L_{SIDE} and simplified n^{++} InGaAs S/D scheme, which is fabricated in this work to improve electrostatics and scalability.

Device Fabrication

Figs. 2(a)-(b) show that the device structures in Figs. 1(b)-(c) exhibit similar capacitance (C) versus voltage (V_G) and transconductance versus V_G characteristics, respectively, indicating that removal of thick upper barrier and Si δ-doping does not affect device performance adversely. In Fig. 3 Transfer length method (TLM) measurements show simplified S/D scheme in this work (Fig. 1(c)) achieves 90% reduction in barrier resistance (R_B) over previous scheme (Fig. 1(b)), while n^{++} cap contact resistance (R_C) remains identical as expected. Cross-section TEM micrograph of the non-planar QWFET in Fig. 4 shows the ultra-scaled L_{SIDE} achieved via the TaSiOx gate dielectric layer. L_{SIDE} is determined by the physical thickness of the gate dielectric layer. This simplified S/D scheme facilitates fabrication of the non-planar multi-gate QWFETs. In Fig. 5(a) C-V_G measurements from 10kHz to 1MHz show minimal frequency dispersion for both TaSiOx/InP and TaSiOx/InGaAs capacitors, suggesting good oxide quality on both the top and the sides of the fin structure. Peak conductance measurements in Fig. 5(b) show low interface trap density D_{it} (in low e11 range) for both TaSiOx/InP and TaSiOx/InGaAs capacitors, although the latter shows 2X higher peak D_{it} value. Figs. 6(a)-(b) show tilted and cross-sectional SEM micrographs, respectively, of the InGaAs non-planar device structures after fin formation using ICP dry etch. In this work three different fin widths (W_{FIN}) are used as shown in Fig. 6(a): 80nm, 60nm and 35nm with fin height (H_{FIN}) =50nm. TEM micrographs in Figs. 7(a)-(b) show two non-planar, multi-gate QWFET device structures with

different fin dimensions after high-K/metal gate formation. To ensure full gating of the entire device, conformal ALD TaSiOx gate dielectric and PVD TiN gate metal are used.

Device Results

The C-V_G of non-planar and planar QWFET structures from the same wafer with T_{OXE}=20.5Å and 21.5Å respectively are compared in Fig. 8(a). The non-planar structure shows healthy C-V characteristics with expected T_{OXE} indicating that the entire InGaAs fin is fully gated. Fig. 8(b) compares the J_G-V_G on the same planar and non-planar QWFET structures. The non-planar QWFET structure shows similarly low J_G as the planar structure, indicating that there is no gate dielectric degradation in the non-planar architecture. Figs. 9(a)-(b) show C-V_G and I_D-V_G data for planar (InGaAs QW thickness of 40nm) and non-planar QWFET structures with H_{FIN}=40nm and three different W_{FIN}=80nm, 60nm and 35nm on the same wafer with L_G=20µm. The data shows: (i) threshold voltage (V_T) increases, i.e. more enhancement mode, with reducing W_{FIN} due to stronger gate control, and (ii) subthreshold slope (SS) is low and similar for all the devices indicating good interface quality for all cases including the (110) InGaAs/high-K interface. The table in Fig. 9(c) summarizes the T_{OXE}, V_T, and SS of all devices in Figs. 9(a)-(b). Fig. 10 shows I_D-V_G of a non-planar QWFET with L_G=70nm, W_{FIN}=60nm, H_{FIN}=50nm, T_{OXE}=20.5Å, and L_{SIDE}=5nm. Figs. 11-12 show the drain induced barrier lowering (DIBL) and SS versus L_G respectively, comparing the planar device (InGaAs QW thickness of 50nm) and non-planar QWFET device with W_{FIN}=60nm and H_{FIN}=50nm. Both planar and non-planar devices have similar T_{OXE}~21Å. The non-planar device shows significant improvement in both DIBL and SS due to more gate control and improved electrostatics. Included in Fig. 12 is the most recent non-planar, multi-gate InGaAs MOSFET [2].

Conclusions

Non-planar, multi-gate InGaAs QWFETs with high-K gate dielectric, ultra-scaled L_{SIDE} of 5nm, and a simplified n^{++} InGaAs source/drain have been fabricated. The high-K gate dielectric formed on this non-planar device structure has the expected thin T_{OXE} of 20.5Å with low J_G, and high quality gate dielectric interface. Compared to the planar high-K InGaAs QWFET with similar T_{OXE}, the non-planar, multi-gate InGaAs QWFET shows (i) more enhancement-mode V_T and (ii) significantly improved electrostatics due to better gate control. The results of this work show that non-planar, multi-gate device architecture is an effective way to improve the scalability of III-V QWFETs for low power logic applications.

References

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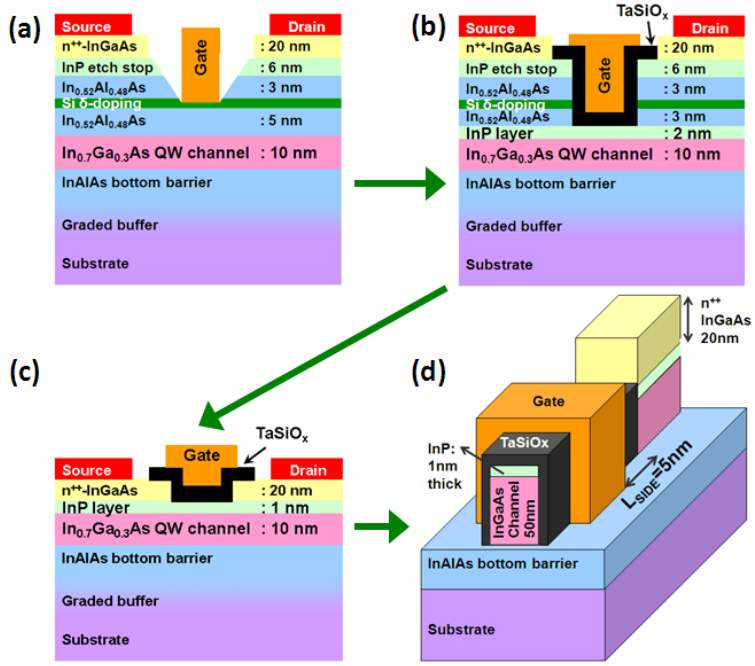

Fig. 1: Evolution of InGaAs QWFET from planar to non-planar, multi-gate architecture: (a) Planar Schottky gate QWFET with source/drain comprised of n^{++} InGaAs cap, thick upper barriers and Si δ-doping [3]. (b) Planar QWFET structure similar to (a) except the Schottky gate is replaced by high-K/metal gate stack [4]. (c) Planar high-K QWFET similar to (b) except the thick upper barriers and Si δ-doping are removed in the S/D area [this work]. (d) Non-planar, multi-gate high-K QWFET, with the transistor channel being in the shape of a "fin", and ultra scaled drain-gate and source-gate separations (L_{SIDE}) [this work]. Eliminating the thick upper barriers and Si δ-doping in (c) and (d) while using n^{++} InGaAs cap as the carrier supply enables S/D contact area scaling with low resistance [5].

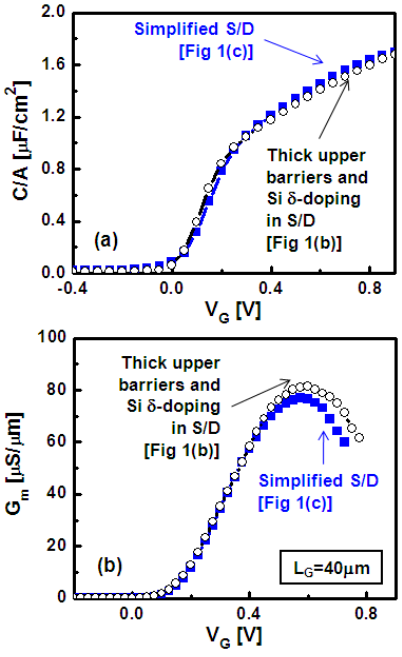

Fig. 2: Device structures in Fig. 1(b) and 1(c) show similar (a) capacitance (C) versus voltage (V_G) and (b) transconductance (Gm) versus V_G characteristics, indicating that removal of thick upper barrier and Si δ-doping does not affect device performance adversely. This simplified S/D structure in Fig. 1(c) enables S/D contact area scaling with low resistance [5] and facilitates fabrication of the non-planar, multi-gate architecture in Fig. 1(d).

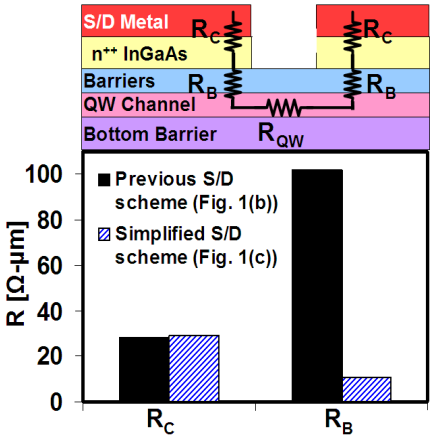

Fig. 3: Transfer length method (TLM) measurements show simplified S/D scheme in this work (Fig. 1(c)) achieves 90% reduction in barrier resistance (R_B) over previous scheme (Fig. 1(b)), while n^{++} cap contact resistance (R_C) remains identical as expected.

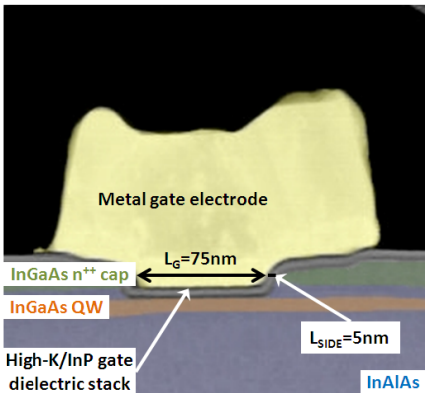

Fig. 4: Cross-section TEM micrograph of the non-planar QWFET showing the ultra-scaled gate-to-source/gate-to-drain separation (L_{SIDE}) achieved via the TaSiOx gate dielectric layer. L_{SIDE} is determined by the physical thickness of the gate dielectric layer.

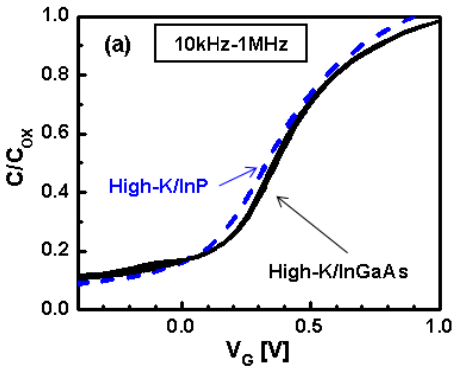

Fig. 5(a): C-V_G measurements from 10kHz to 1MHz show minimal frequency dispersion for both high-K/InP and high-K/InGaAs capacitors, with good oxide quality on both substrates. The high-K gate dielectric is TaSiOx. The data suggests good oxide quality on both the top and the sides of the fin structure.

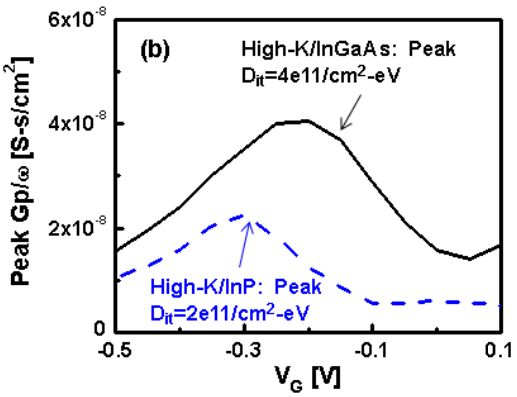

Fig. 5(b): Peak conductance measurements show low interface trap density, D_{it} (in low e11 range) for both high-K/InP and high-K/InGaAs capacitors, although the latter shows 2X higher peak D_{it} value.

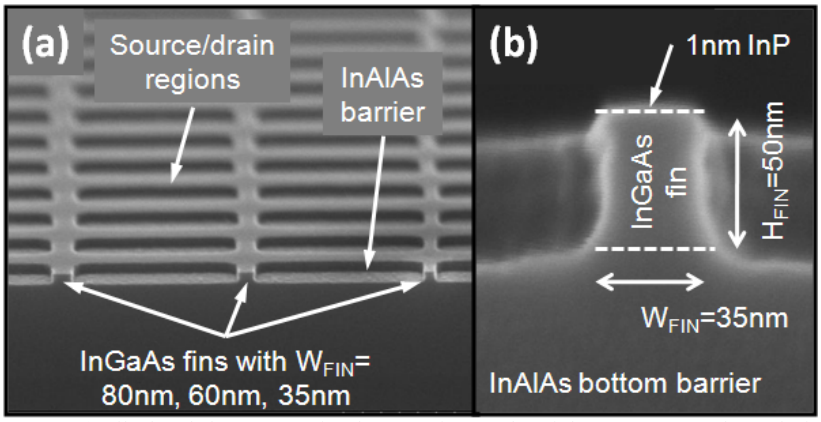

Fig. 6: (a) Tilted and (b) cross-sectional SEM micrographs of the InGaAs non-planar device structures after fin formation. In this work three different fin widths (W_{FIN}) are used as shown in (a): 80nm, 60nm and 35nm. Fig. 6(b) shows an InGaAs fin structure with W_{FIN}=35nm and fin height (H_{FIN}) =50nm.

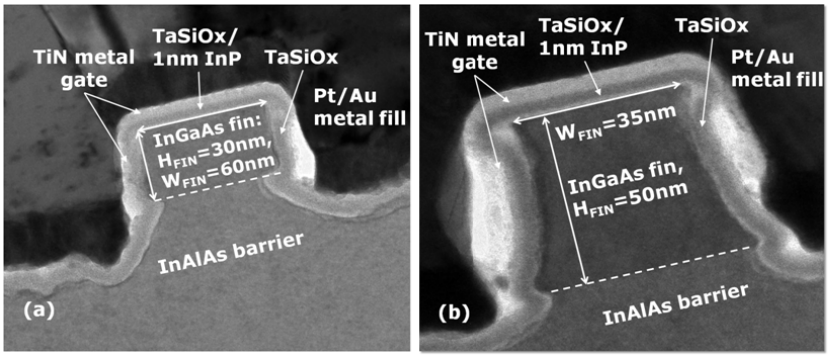

Fig. 7(a)-(b): TEM micrographs of two non-planar, multi-gate InGaAs QWFET device structures with different fin dimensions after high-K/metal gate formation. To ensure full electrical gating of the entire device, conformal ALD TaSiOx gate dielectric and PVD TiN gate metal are used.

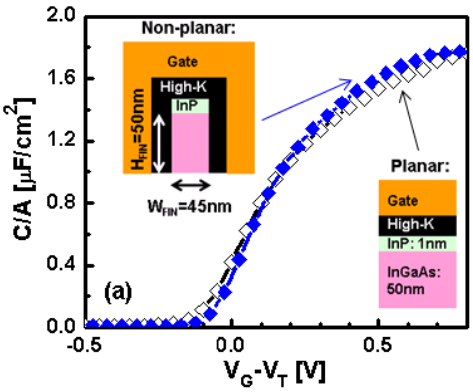

Fig. 8(a): C-V_G measurements made on the planar and non-planar QWFET structures on the same wafer with same simplified n^{++} InGaAs S/D. The non-planar and planar structures have T_{OXE}=20.5Å and 21.5Å respectively. Similar to the planar structure, the non-planar structure shows healthy C-V characteristics with expected T_{OXE} indicating that the entire InGaAs fin is fully gated.

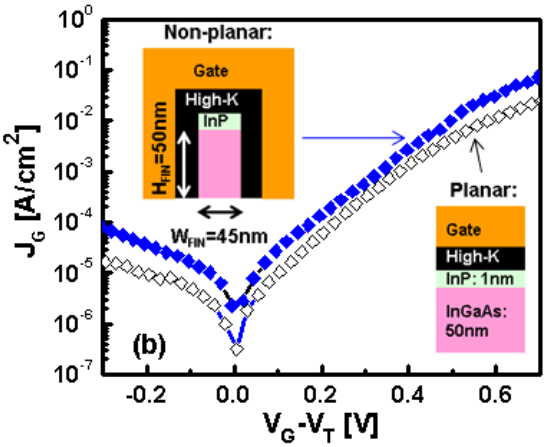

Fig. 8(b): Gate dielectric leakage (J_G) versus V_G measurements made on the planar and non-planar QWFET structures as shown in Fig. 8(a). The non-planar QWFET structure shows similarly low J_G as the planar structure, indicating that there is no gate dielectric degradation in the non-planar architecture.

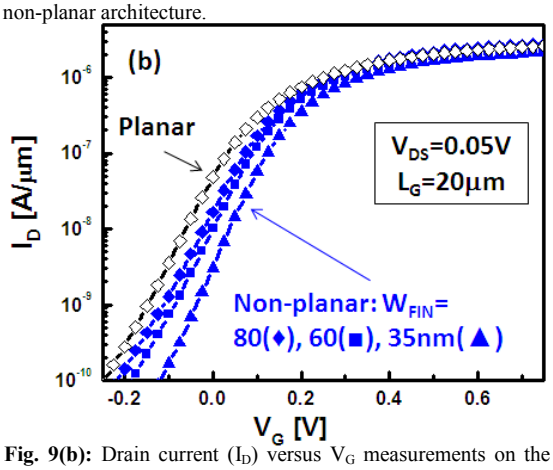

Fig. 9(b): Drain current (I_D) versus V_G measurements on the same planar and non-planar QWFET structures as in Fig. 7(a). The data shows: (i) transistor threshold voltage (V_T) increases, i.e. more enhancement mode, with reducing W_{FIN} due to stronger gate control, and (ii) subthreshold slope (SS) is low and similar for all the devices indicating good interface quality for all cases including the (110) InGaAs/high-K interface on both sides of the fin of the non-planar devices.

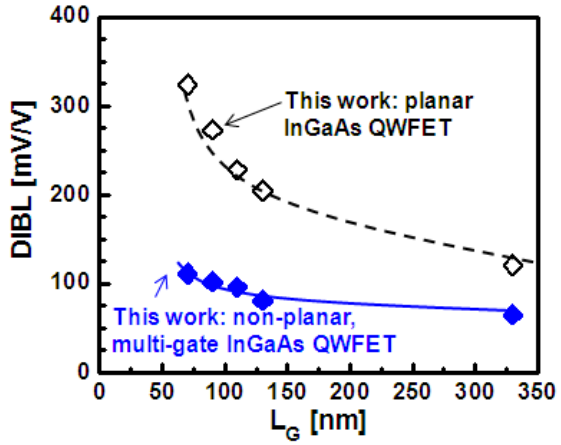

Fig. 11: Drain induced barrier lowering (DIBL) versus L_G comparing the planar device (InGaAs QW thickness of 50nm) and non-planar, multi-gate QWFET device with W_{FIN}=60nm and H_{FIN}=50nm. Comparing to the planar device, the non-planar device shows significant improvement in DIBL due to improved electrostatics.

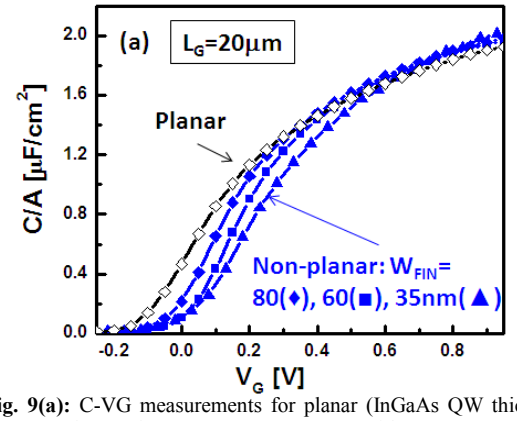

Fig. 9(a): C-VG measurements for planar (InGaAs QW thickness of 40nm) and non-planar QWFET structures with H_{FIN}=40nm and three different W_{FIN}=80nm, 60nm and 35nm on the same wafer. All devices have long channel L_G=20µm. Similar to the planar structure, all three non-planar structure shows healthy C-V characteristics with expected T_{OXE} indicating that the entire InGaAs fin is fully gated.

Fin width	T_{OXE} (Å)	V_T (V)	SS (mV/dec)
planar	21.6	0.02	73
80nm	20.3	0.075	77
60nm	20.5	0.09	77
35nm	20.7	0.12	75

Fig. 9(c): Table summarizes the T_{OXE}, V_T, and SS of all devices in Fig. 9(a)-(b) for long channel L_G=20µm.

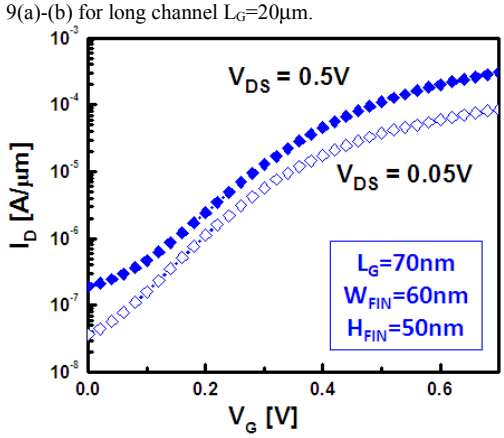

Fig. 10: I_D-V_G of a non-planar, multi-gate InGaAs QWFET with L_G=70nm, W_{FIN}=60nm, H_{FIN}=50nm, T_{OXE}=20.5Å, and L_{SIDE}=5nm.

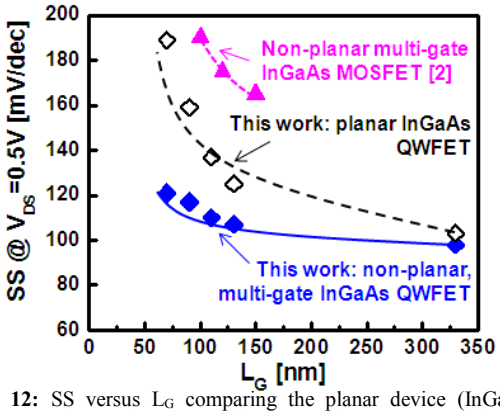

Fig. 12: SS versus L_G comparing the planar device (InGaAs QW thickness of 50nm) and non-planar, multi-gate QWFET device with W_{FIN}=60nm and H_{FIN}=50nm. The devices have T_{OXE}~21Å and ultra-scaled L_{SIDE} of 5nm. Comparing to the planar device, the non-planar device shows significant improvement in SS due to improved electrostatics. Included is the most recent non-planar, multi-gate InGaAs MOSFET device from Ref. [2].