

Intel® 7510/7512 Scalable Memory Buffer

Specification Update

April 2011

Notice: The Intel® 7510/7512 Scalable Memory Buffer may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Reference Number: 325123-001



INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

Intel products are not intended for use in medical, life saving, life sustaining, critical control or safety systems, or in nuclear facility applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

The Intel® 7510/7512 Scalable Memory Buffer may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are available upon request.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

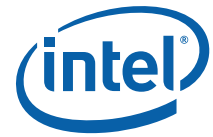
Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an order number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at <http://www.intel.com>.

Intel, Xeon, Itanium, and the Intel logo are trademarks of Intel Corporation in the U. S. and other countries.

*Other names and brands may be claimed as the property of others.

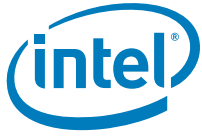
Copyright © 2011, Intel Corporation. All Rights Reserved.

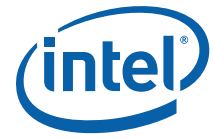


Contents

Revision History	5
Preface	6
Summary Table of Changes	7
Errata Summary	8
Identification Information	9
Errata	10
Documentation Changes/Clarifications	12

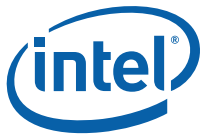
§





Revision History

Revision Number	Description	Date
001	<ul style="list-style-type: none"><li data-bbox="561 495 878 520">• Initial release of the document.	April, 2011



Preface

This document is an update to the specifications contained in the Affected Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents

Document Title	Document Number/ Location
Intel® 7500/7510/7512 Scalable Memory Buffer Datasheet	322824/http:// www.intel.com

Related Documents

Document Title	Location
JESD79-3 DDR3 SDRAM Specification	JEDEC

Nomenclature

Errata are design defects or errors. These may cause the Intel® 7510/7512 Scalable Memory Buffer's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note:

Errata remain in the Specification Update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, and so forth.).



Summary Table of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to Intel® 7510/7512 Scalable Memory Buffer. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Stepping

- X: A sighting exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
- (No mark) or (Blank box): This sighting is fixed in listed stepping or specification change does not apply to the listed stepping.

Platform

- X: A X, in the Intel® Itanium® processor 9300 series-based platform indicates the Intel® 7510/7512 Scalable Memory Buffer sighting exists in the Intel® Itanium® processor 9300 series-based platform. A X, in the Intel® Xeon® processor 7500 series-based platform indicates the Intel® 7510/7512 Scalable Memory Buffer sighting exists in the Intel® Xeon® processor 7500 series-based platform.
- (Blank box): This sighting does not apply to the platform.

Page

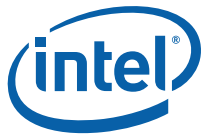
- (Page): Page location of item in this document.

Status

- Doc: Document change or update will be implemented.
- Plan Fix: This sighting may be fixed in a future stepping of the product. Plan Fix (HW) indicates that the fix will be implemented in silicon.
- Fixed: This sighting has been previously fixed.
- No Fix: There are no plans to fix this sighting.
- Under Investigation: The disposition of this sighting has not been determined. An "Under Investigation" status will be updated in a future release of this document.

Row

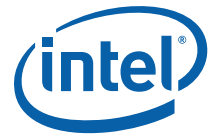
- | Change bar on outside margins indicates this sighting is either new or modified from the previous version of the document.



Errata Summary

Table 1. Errata Summary Table

#	Stepping		Status	CPU	Errata
	A0	A1		Intel® Xeon® Processor E7-8800/4800/2800 Product Families	
1.	X	X	No Fix	X	On Intel® 7510/7512 Scalable Memory Buffer, JTAG - BScan EXTEST is non-compliant to 1149.1 specification (uses wrong clock edge).
2.	X	X	No Fix	X	During an Intel® SMI Disable_b event, SMBus transactions underway between bus Master and another device on the bus other than Intel® 7510/7512 Scalable Memory Buffer may be affected.
3.	X	X	No Fix	X	Broken trace to either the P or the N lane of the Intel® SMI forwarded clock differential pair may result in loss of forwarded clock but not always lead to clock lane failover.
4.	X	X	No Fix	X	Under cold operating conditions, manufacturing stress tests reveal issues with Intel® 7510 Scalable Memory Buffer (Standard SKU; maxTDP=8.7W) s-spec parts.



Identification Information

Component Identification via Programming Interface

The Intel® 7510/7512 Scalable Memory Buffer stepping can be identified by the following register contents:

Stepping	Features	Vendor ID	Device ID	Revision Number
A1	Engineering Sample 2	8086h	0881h	01h

Component Marking Information

The Intel® 7510 Scalable Memory Buffer stepping can be identified by the following component markings:

Stepping	Top Marking	Notes
A1	BD82030M2	MM#: 908098
A1	BD7510	MM#: 910394

The Intel® 7512 Scalable Memory Buffer stepping can be identified by the following component markings:

Stepping	Top Marking	Notes
A1	BD82029M2	MM#: 908099
A1	BD7512	MM#: 910395



Errata

1. On Intel® 7510/7512 Scalable Memory Buffer, JTAG - BScan EXTEST is non-compliant to 1149.1 specification (uses wrong clock edge).

Problem: As per the JTAG 1149.1 specification, “test data registers enabled to drive data off-chip shall be designed such that component outputs change only on the **falling** edge of TCK after entry to the Update-DR, Update-IR, Run-Test/Idle or Test-Logic-Reset controller state as a result of signals applied to TCK and TMS”. Intel® 7510/7512 Scalable Memory Buffer is in violation of this specification.

Implication: On Intel® 7510/7512 Scalable Memory Buffer, while performing DfX Boundary Scan (EXTEST), system pins (including DDR, Intel® Scalable Memory Interconnect (Intel® SMI) and misc IOs) are transmitted on the **rising** TCK edge (instead of falling TCK edge).

Workaround: If using automated test equipment to sample the output data when executing EXTEST, the test must wait for the rising edge of TCK before sampling the values being driven on the Intel® 7510/7512 Scalable Memory Buffer output pins.

Status: No Fix.

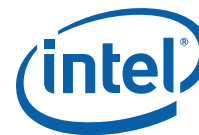
2. During an Intel® SMI Disable_b event, SMBus transactions underway between bus Master and another device on the bus other than Intel® 7510/7512 Scalable Memory Buffer may be affected.

Problem: Intel® 7510/7512 Scalable Memory Buffer EDS (rev1.9) states that SMBus transactions to the memory buffer that are underway during an Intel® SMI Disable_b event may not complete normally. In addition, SMBus transactions underway to devices other than Intel® 7510/7512 Scalable Memory Buffer may also be affected. For example, a transaction underway to a DIMM Thermal Sensor (TS) during a Disable_b event may result in Intel® 7510/7512 Scalable Memory Buffer interpreting the SMBus transaction as targeting that memory buffer. If this occurs then Intel® 7510/7512 Scalable Memory Buffer can mistakenly drive the SMBus, even though it is not the target device.

Implication: Disable_b events can occur as a result of a CRC error handling routine, or as part of the Intel® SMI link-down memory self-refresh power saving mode. Under this specific error event, Intel® 7510/7512 Scalable Memory Buffer can drive SMBus for one or more clocks, resulting in corruption of the transaction in progress. If the transaction results in data corruption, and has Parity Error Checker (PEC) enabled, the error will be detected by the master or slave, and then the transaction can be retried. If PEC is not enabled then some other mechanism will be needed to ensure integrity of the transaction. It is also possible that the transaction request will time out.

Workaround: At Intel, this sighting was observed when continuously polling the DIMM Thermal Sensor (TS) as part of fan speed control mechanism. The observed failure rate was very low for this specific usage model. In this case, as workaround, a modified algorithm can perform multiple reads and filter ‘outlier values’ before consuming the data. On usage models that involve SMBus writes, a read-after-write from the same target address would be needed to confirm the integrity of the write data. It is not recommended to do Block Read/Write transactions (e.g to DIMM SPD for error logging) since large data transfers create a probability that a specific pattern could occur which matches Intel® 7510/7512 Scalable Memory Buffer’s target address followed by a write command, and could be consumed by Intel® 7510/7512 Scalable Memory Buffer. This has not been observed at Intel, but is a theoretical possibility. Limiting SMBus transfers to less than 8 bytes between Start/Stop bits, eliminates this as a possibility. (DIMM Thermal Sensor polling is a 5 byte SMBus transaction).

Workarounds are dependent on customer specific usage models. Customers will likely wish to test their own transaction corruption rate. Customers should work with Intel to implement workarounds for other usage models.



Status: No fix.

3. Broken trace to either the P or the N lane of the Intel® SMI forwarded clock differential pair may result in loss of forwarded clock but not always lead to clock lane failover.

Problem: If either only the P or the N lane of the Intel® SMI forwarded clock is broken, then Intel® 7510/7512 Scalable Memory Buffer is capable of detecting minimum differential swing on the clock lane, thus resulting in the memory buffer to assume that the forwarded clock still exists. Consequently, Intel® 7510/7512 Scalable Memory Buffer will proceed to the Intel® SMI link training phase.

Implication: If Intel® 7510/7512 Scalable Memory Buffer proceeds to the link training phase, then based on observations, it is possible that the Intel® SMI link may fail to train even after seven retry attempts and continue to remain in RESET state; or, if the link successfully reached L0 state, then the link may be unstable and shortly return to Disable_a state. However, if the P and N lanes of the forwarded clock differential pair are both broken due to board trace issues, then the clock failover mechanism on Intel® SMI channel has been found to operate successfully as expected.

Workaround: None exists at the moment.

Status: No Fix.

4. Under cold operating conditions, manufacturing stress tests reveal issues with Intel® 7510 Scalable Memory Buffer (Standard SKU; maxTDP=8.7W) s-spec parts.

Problem: Under cold temperature (<10C) and low Vcc1P1 (~1.087V) settings during manufacturing testing, Intel® 7510 Scalable Memory Buffer s-spec parts have been observed to cause system issues. Symptoms appear as North-bound or South-bound CRC errors while attempting to boot OS. Not all Intel® 7510 Scalable Memory Buffer s-spec parts cause these system issues. Additionally, operating condition must include both cold temperature and low Vcc1P1.

Implication: Intel® 7510 Scalable Memory Buffer Qualification samples do not exhibit this problem. Additionally, it is not possible to identify which Intel® 7510 Scalable Memory Buffer s-spec parts may cause this problem under cold operating and low Vc1P1 conditions. As a result, a system using Intel® 7510 Scalable Memory Buffer s-spec parts is at risk of running into OS boot-up issues.

Workaround: To avoid running into the cold socket issue with production units, the workaround consists of 2 steps, both being required: (

1) minor change in the MRC, starting with RC1.9

2) raising by 10mV the specification of the digital and analog 1.1 V rail inputs to the Intel® 7510 Scalable Memory Buffer

Note: Intel® 7512 Scalable Memory Buffer (low power SKU; maxTDP=6.5W) is not exposed to this issue; hence there is no change to 1.1 V input specification for Low Power SKU.

Status: No silicon fix.



Documentation Changes/ Clarifications

1. Intel® 7510/7512 Scalable Memory Buffer behavior in the event of loss of South bound forwarded clock during Disable_a state.

Intel® 7510/7512 Scalable Memory Buffer can not tell the difference between a SB forwarded clock failure due to signal integrity issues, and the deliberate use of the SMI Disable_a state for power management by the host memory controller. After the SB forwarded clock is stopped by the host, Intel® 7510/7512 Scalable Memory Buffer will flag an error in FERR/NERR.SBFWCLK, if EMASK.SBFWCLK is set to '0'. If the SMI Disable_a state is used for power management, it is up to the host to mask this error, clear this error, or ignore this error.